

CLAIMS

What is claimed is:

- 1 1. A back illuminated photodiode array comprising:
2 a substrate of a first conductivity type having first
3 and second surfaces;
4 the second surface having a layer of the first
5 conductivity type having a greater conductivity than the
6 substrate;
7 a matrix of regions of a first conductivity type of a
8 higher conductivity than the substrate extending from the
9 first surface of the substrate to the layer of the first
10 conductivity type having a greater conductivity than the
11 substrate;
12 a plurality of regions of the second conductivity type
13 interspersed within the matrix of regions of the first
14 conductivity type and not extending to the layer of the first
15 conductivity type on the second surface of the substrate;
16 and,
17 a plurality of contacts on the first surface for making
18 electrical contact to the matrix of regions of the first
19 conductivity type and the plurality of regions of the second
20 conductivity type.

1 2. The photodiode array of claim 1 wherein the
2 plurality of regions of the second conductivity type are
3 separated from the second surface of the substrate by an
4 amount that approximately equals the depletion depth for the
5 substrate at zero bias.

1 3. The photodiode array of claim 1 wherein the
2 plurality of regions of the second conductivity type are
3 separated from the second surface of the substrate by
4 approximately 9 μm .

1 4. The photodiode array of claim 2 wherein the
2 substrate is an n-type silicon substrate having a resistivity
3 of approximately 400 ohm-cm.

1 5. The photodiode array of claim 1 wherein the
2 plurality of contacts are a plurality of ball grid contacts.

1 6. The photodiode array of claim 5 wherein the
2 plurality of contacts are of substantially equal size evenly
3 distributed across the photodiode array.

1 7. The photodiode array of claim 1 wherein the matrix
2 of regions of a first conductivity type comprise a
3 rectangular matrix defining an X-Y matrix of square regions,

4 each square region containing a respective one of the
5 plurality of regions of the second conductivity type.

1 8. The photodiode array of claim 7 wherein doping
2 forming the matrix of regions of a first conductivity type
3 and the plurality of regions of the second conductivity type
4 overlap.

1 9. The photodiode array of claim 1 wherein the
2 substrate has a thickness of less than approximately 50 μm .

1 10. The photodiode array of claim 1 wherein the
2 substrate has a thickness of approximately 30 μm .

1 11. The photodiode array of claim 1 wherein the
2 substrate is a silicon substrate.

1 12. A back illuminated photodiode array comprising:
2 a substrate of a first conductivity type having first
3 and second surfaces and a thickness of less than
4 approximately 50 μm ;

5 the second surface having a layer of the first
6 conductivity type having a greater conductivity than the
7 substrate;

8 a rectangular matrix of regions of a first conductivity
9 type of a higher conductivity than the substrate extending
10 from the first surface of the substrate to the layer of the

11 first conductivity type on the second surface of the
12 substrate, the rectangular matrix defining an X-Y matrix of
13 rectangular regions;

14 a plurality of regions of the second conductivity type
15 interspersed within the matrix of regions of the first
16 conductivity type, each region of the second conductivity
17 type being within a respective square region defined by the
18 rectangular matrix of regions of a first conductivity type;
19 and,

20 a plurality of contacts on the first surface for making
21 electrical contact to the matrix of regions of the first
22 conductivity type and the plurality of regions of the second
23 conductivity type.

1 13. The photodiode array of claim 12 wherein the
2 plurality of regions of the second conductivity type are
3 separated from the second surface of the substrate by an
4 amount that approximately equals the depletion depth for the
5 substrate at zero bias.

1 14. The photodiode array of claim 13 wherein the
2 plurality of regions of the second conductivity type are
3 separated from the second surface of the substrate by
4 approximately 9 μm .

1 15. The photodiode array of claim 13 wherein the
2 substrate is an n-type silicon substrate having a resistivity
3 of approximately 400 ohm-cm.

1 16. The photodiode array of claim 12 wherein the
2 plurality of contacts are a plurality of ball grid contacts.

1 17. The photodiode array of claim 16 wherein the
2 plurality of contacts are of substantially equal size
3 substantially evenly distributed across the photodiode array.

1 18. The photodiode array of claim 12 wherein doping
2 forming the matrix of regions of a first conductivity type
3 and the plurality of regions of the second conductivity type
4 overlap.

1 19. The photodiode array of claim 12 wherein the
2 substrate has a thickness of approximately 30 μm .

1 20. The photodiode array of claim 12 wherein the
2 substrate is a silicon substrate.

1 21. A method of fabricating a photodiode array
2 comprising:
3 providing a semiconductor substrate having first and
4 second surfaces;

5 providing a first region in the form of a matrix of
6 regions of a first conductivity type of a higher conductivity
7 than the substrate, including a high temperature diffusion,
8 the first region extending into the substrate from the first
9 surface;

10 providing a plurality of regions of the second
11 conductivity type interspersed within the matrix of regions
12 of the first conductivity type, including an additional high
13 temperature diffusion, the second region extending into the
14 substrate from the first surface a shorter distance than the
15 first region;

16 grinding the substrate from the second surface to reduce
17 the thickness of the substrate and to expose the matrix of
18 regions of a first conductivity type and not the plurality of
19 regions of the second conductivity type at the second surface
20 of the substrate;

21 providing a layer of the first conductivity type having
22 a conductivity greater than the substrate on the second
23 surface of the substrate; and,

24 providing a plurality of electrical contacts at the
25 first surface for the first region in the form of a matrix of
26 regions of a first conductivity type and the plurality of
27 regions of the second conductivity type.

1 22. The method of claim 21 wherein the layer of the
2 first conductivity type having a conductivity greater than
3 the substrate on the second surface of the substrate is
4 provided by implantation.

1 23. The method of claim 21 wherein the substrate is
2 ground to a thickness separates the plurality of regions of
3 the second conductivity type from the second surface of the
4 substrate by an amount that approximately equals the
5 depletion depth for the substrate at zero bias.

1 24. The photodiode array of claim 21 wherein the
2 plurality of regions of the second conductivity type are
3 separated from the second surface of the substrate by
4 approximately 9 μm .

1 25. The method of claim 23 wherein the substrate
2 provided is an n-type silicon substrate having a resistivity
3 of approximately 400 ohm-cm.

1 26. The method of claim 21 wherein the plurality of
2 contacts are a plurality of ball grid contacts.

1 27. The method of claim 26 wherein the plurality of
2 contacts are of substantially equal size evenly distributed
3 across the photodiode array.

1 28. The method of claim 21 wherein the substrate is
2 ground to a thickness of less than approximately 50 μm .

1 29. The method of claim 21 wherein the substrate is
2 ground to a thickness of approximately 30 μm .

1 30. A method of fabricating a photodiode array
2 comprising:

3 providing a silicon substrate having first and second
4 surfaces;

5 providing a first region in the form of a matrix of
6 regions of a first conductivity type of a higher conductivity
7 than the substrate, including a high temperature diffusion,
8 the first region extending into the substrate from the first
9 surface;

10 providing a plurality of regions of the second
11 conductivity type interspersed within the matrix of regions
12 of the first conductivity type, including an additional high
13 temperature diffusion, the second region extending into the
14 substrate from the first surface a shorter distance than the
15 first region;

16 providing additional doping of the first region,
17 including a further high temperature diffusion;

18 grinding the substrate from the second surface to reduce
19 the thickness of the substrate to less than approximately 50

20 μm and to expose the matrix of regions of a first
21 conductivity type and not the plurality of regions of the
22 second conductivity type at the second surface of the
23 substrate;

24 providing a layer of the first conductivity type having
25 a conductivity greater than the substrate on the second
26 surface of the substrate; and,

27 providing a plurality of electrical contacts at the
28 first surface for the first region in the form of a matrix of
29 regions of a first conductivity type and the plurality of
30 regions of the second conductivity type.

1 31. The method of claim 30 wherein the layer of the
2 first conductivity type having a conductivity greater than
3 the substrate on the second surface of the substrate is
4 provided by implantation.

1 32. The method of claim 30 wherein the substrate is
2 ground to a thickness that separates the plurality of regions
3 of the second conductivity type from the second surface of
4 the substrate by an amount that approximately equals the
5 depletion depth for the substrate at zero bias.

1 33. The photodiode array of claim 30 wherein the
2 plurality of regions of the second conductivity type are

3 separated from the second surface of the substrate by
4 approximately 9 μm

1 34. The method of claim 32 wherein the substrate
2 provided is an n-type silicon substrate having a resistivity
3 of approximately 400 ohm-cm.

1 35. The method of claim 30 wherein the plurality of
2 contacts are a plurality of ball grid contacts.

1 36. The method of claim 35 wherein the plurality of
2 contacts are of substantially equal size evenly distributed
3 across the photodiode array.

1 37. The method of claim 30 wherein the substrate is
2 ground to a thickness of approximately 30 μm .

1 38. A method of fabricating a semiconductor device
2 comprising:

3 providing a semiconductor substrate of a first
4 conductivity type;

5 forming the semiconductor device on a first surface of
6 the semiconductor substrate, including forming deep
7 diffusions extending through the substrate from the first
8 surface to a second surface of the substrate; and,

9 forming a blanket region of the same conductivity type
10 as the deep diffusions on the second surface of the
11 substrate.

1 39. The method of claim 38 wherein the substrate is of
2 a first conductivity type and the deep diffusions and the
3 blanket region are of a second conductivity type.

1 40. The method of claim 38 wherein the deep diffusions
2 extending through the substrate are formed by forming
3 diffusions that are deeper than diffusions of the
4 semiconductor device, and grinding the substrate from the
5 second surface to reduce the thickness of the substrate to
6 expose the deep diffusions from the second surface of the
7 substrate.

1 41. A method of fabricating a semiconductor device
2 comprising:

3 providing a semiconductor substrate of a first
4 conductivity type; and,

5 forming the semiconductor device on a first surface of
6 the semiconductor substrate, including forming deep
7 diffusions extending through the substrate from the first
8 surface to a second surface of the substrate.

1 42. The method of claim 41 wherein the deep diffusions
2 extending through the substrate are formed by forming
3 diffusions that are deeper than diffusions of the
4 semiconductor device but do not extend through the substrate,
5 and grinding the substrate from the second surface to reduce
6 the thickness of the substrate to expose the deep diffusions
7 from the second surface of the substrate.